14.1 A 90nm CMOS Low-Power GSM/EDGE Multimedia-Enhanced Baseband Processor with 380MHz ARM9 and Mixed-Signal Extensions

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Modern baseband ICs require increasing data processing capabilities for modem functionality and various multimedia features [1]. The presented baseband IC (BB-IC) has a classical dual core architecture composed of an ARM926 MCU and a TEAKlite DSP communicating via shared memory. Together with a carefully selected set of multimedia extensions and integrated analog/mixed signal features this chip facilitates a cost-effective solution for 2.5G feature phones. Furthermore, the modem functionality can be enhanced up to UMTS and HSDPA with a L1 co-processor chip, which satisfies the need for simple scalability. Due to the limited power budget, the development of a BB-IC demands system and circuit level co-design as well as an appropriate partition of digital and analog functionalities. Additionally, the use of sub-100nm CMOS technologies necessitates a trade-off between performance and leakage currents.

A top-down approach is followed to derive the optimum system architecture and circuit implementation from the specific requirements of relevant applications. The table in Fig. 14.1.1 summarizes throughput requirements in terms of clock frequencies for the various cores and components. HSDPA data transfer at 3.6Mb/s requires very high performance for the ARM, whereas the DSP is idle. Video applications require high performance for both, ARM and DSP, while for the GSM modes and MP3 replay a much lower performance is sufficient. After analyzing the activities of the cores, a grouping of the components into independent switch domains is performed to implement the sleep transistor concept for leakage reduction during stand-by periods. The block diagram (Fig. 14.1.2) shows the power supply concept and seven major switch domains for the cores and memories. The standby domain, which includes the system control for handling the reactivation of the core domains, is always active, but operates at only 32kHz during standby mode.

Multi-V_T and multi-gate oxide techniques in our 90nm low power CMOS technology [2,4] are applied in this SoC together with various low power circuit techniques. To address the peak performance requirements all performance relevant cores and sub-blocks contain fully scaled 90nm regular V_T core devices (RVT) with a thin 1.6nm gate oxide. The significant gate leakage contribution of these RVTs is negligible in active mode and eliminated in stand-by mode by applying the sleep transistor concept using a low leakage nFET (LLD) with small leakage currents (5pA/µm at 25˚C). Leakage sensitive circuits such as the standby domain, SRAMs and ROMs are implemented with LLDs to achieve low leakage even in active mode.

Figure 14.1.3 shows the implementation of the nFET sleep-transistor (ST) concept in 90nm CMOS technology with a triple-well implant [2]. Main advantages of nFET sleep transistors compared to pFETs [3,6] are the higher conductance in active mode which results in a 50% lower area overhead for the switches. The benefit of this implementation methodology is that the leakage current is negligible compared to the active power consumption of the standby domain, which uses solely LLDs. A triple well process allows for a substrate isolation of different circuit blocks. This is essential for nFET STs since all internal nodes of a block including the virtual ground and the nFET body potential are floating during standby-mode. Concerning integration of the analog components, the triple well option is advantageous for isolation of sensitive analog circuits from noise generating digital parts. This allows the implementation of a 16b HiFi-stereo audio front-end interface including headset drivers.

To reduce memory access and to enable a fast reactivation after standby, data can be stored locally in switched off domains using retention flip flops (R-FF) [5]. Figure 14.1.4 shows a new implementation of an R-FF using a modified Sense-Amplifier (SA) based flip flop. The SA and the capturing Reset-Set (RS) latch are implemented in fast RVT devices, while the retention part contains LL devices. The transmission gates isolate the retention cell after switching off the sleep transistor. In standby mode this R-FF consumes less than 10pA leakage. Since the retention functionality is usually required only for a small fraction of data, the area overhead of 35%, compared to SA FF's without retention functionality, is acceptable.

The ARM9 core is the component with maximum specified performance requirement of 254MHz. The measurement of the achievable maximum performance is done by using a test pattern which sensitizes the critical path of the respective component. Figure 14.1.5 shows the maximum clock frequency versus V_{DD} for the ARM9 core, the AMBA high speed bus (AHB) and the DSP; the AHB frequency is half of the ARM9 frequency. To address the overall system performance, the maximum frequency of the combined operation of ARM, AHB and external memory controller is also included. At 1.4V, the ARM9 achieves a frequency of 380MHz under nominal process conditions. An evaluation of a split lot shows a variation of f_{max} by about ±10% for the slow and fast process split. Assuming a nominal V_{DD} of 1.35V for the fast mode, the ARM frequency of 360MHz complies with the target values and leaves substantial headroom for additional applications.

To address the application dependent performance requirements of the cores, voltage scaling (VS) in combination with frequency scaling is implemented. Especially in the feature phone market segment the majority of use cases are low performance applications (e.g. speech calls, MP3 playback, etc.). Therefore, high energy efficiency is essential to achieve long battery run times. For the optimum adaptation to the applications, 20 coarse frequency steps are available with additionally fine tuning capability. Figure 14.1.6 shows exemplary power measurements obtained for the ARM core running the Dhrystone 2.1 benchmark. Compared to the fast mode at 254MHz, the slow mode operation at 130MHz allows a power reduction by 52% and 30% due to frequency and voltage scaling, respectively. The excellent low voltage performance is facilitated by the multi-V_T and multi-gate oxide devices. The power consumption for GSM voice calls is below 70mW, comprising the digital and analog mixed-signal contributions. The chip is shown in Fig. 14.1.7 with the various domains indicated.

References:

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[2] T. Schafbauer et al., "Integration of High-performance, Low-leakage and Mixed Signal Features into a 100nm CMOS Technology," *Symp. on VLSI Technology*, pp. 62-63, 2002.
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Application	Settings (resolution, protocol)	µC ARM926 f (MHz)*	DSP TEAKlite f (MHz)*	COMBO**	Peripheral Bus 1	Peripheral Bus 2	Analog	Standby Domain
GSM Voice call	6.60-AMR 6.60-AMR w/ handsfree	26 26	52 65	on	off	off	on	on
GSM idle	sleep mode paging	0 26	0 26	off on	off off	off off	off on	on on
Data download	HSDPA 3.6Mbps UMTS PS 384 kb/s E-GPRS	130 52 52	0 0 104	on	on (MMC IF)	off	off off on	on
Video encode	MPEG-4 (20 fps, QVGA)	254	52	on	on	on	on (audio)	on
Video telephony	MPEG-4 (15 fps, QCIF, UMTS CS)	104	78	on	on	on	on	on
Music replay	MP3 MP3 during paging	26 52	26 26	on	off	off	on	on

* Memory configuration: Cache enabled, Code execution from external SDRAM
** COMBO: ARM & AMBA High Speed Bus & Memory Controller

Figure 14.1.1: Representative set of applications with corresponding throughput requirements.

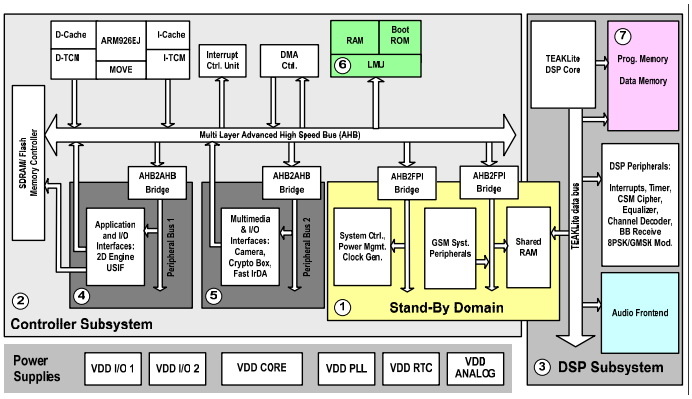


Figure 14.1.2: Chip block diagram with independent power domains shaded differently.

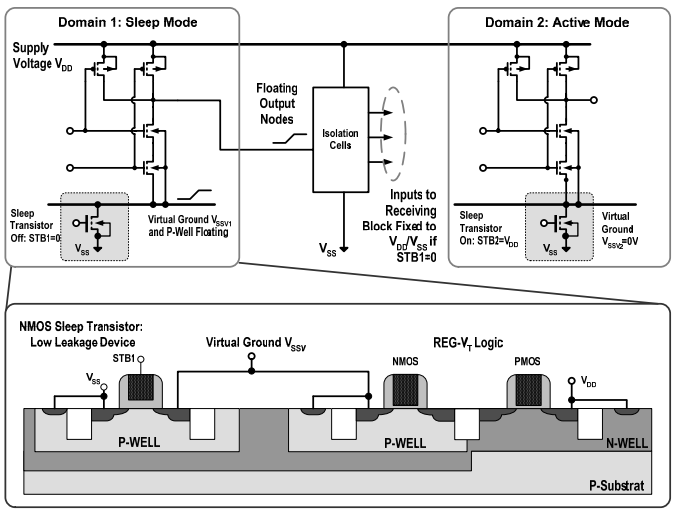
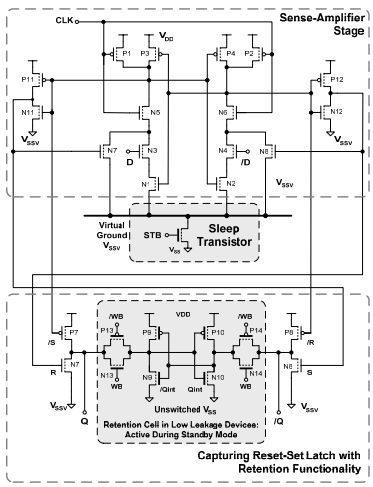


Figure 14.1.3: NMOS sleep transistor implementation in 90nm triple-well CMOS technology.



Active Mode WB=STB=1

- SA input stage generates a pulse to switch Reset-Set (RS) latch
- Fast push-pull devices (P7/N7, P8/N8) provide driving current for small CLK-Q delay
- Retention-FF (R-FF) acts as RS Stage

Standby Mode WB=STB=0

- R-cell is isolated from SA stage and push pull devices
- Transmission gates protect storage nodes (Q_{int}, $/Q_{int}$) and eliminate leakage from push-pull devices

Figure 14.1.4: Retention flip flop implemented in dual gate-oxide/dual-V_T technique.

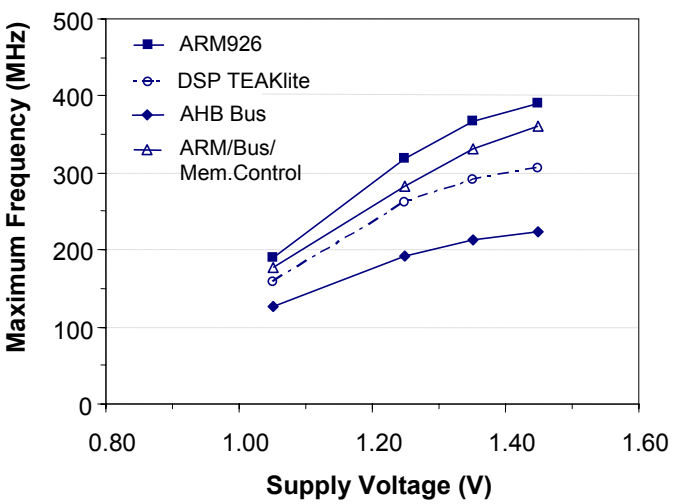


Figure 14.1.5: Measured performance versus V_{DD} for several sub-systems.

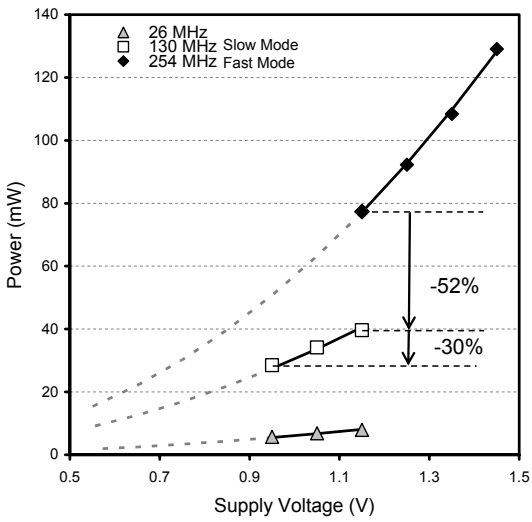


Figure 14.1.6: Measured power dissipation of the ARM926 with frequency and voltage scaling.

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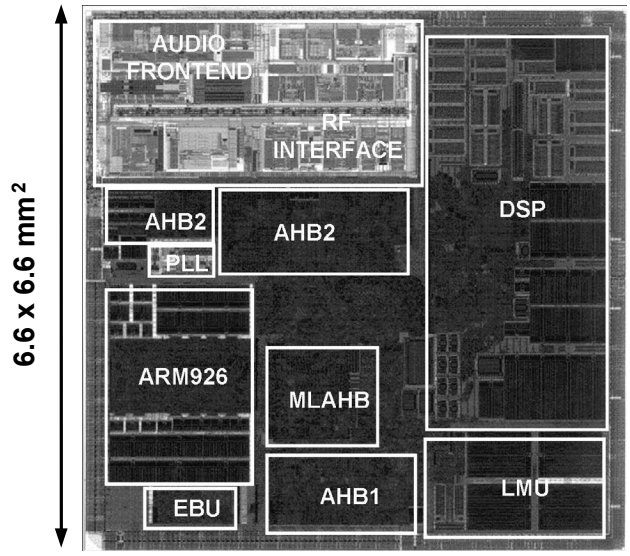

Figure 14.1.7: Chip micrograph.

